Form PTO-1449 (modified) List of Patents and Publications For Applicant's Information Disclosure Statement (Use several sheets if necessary)	ATTY. DKT. NO. 5181-96200 APPLICANT: Cavanagh, et al. FILING DATE: November 9, 2001	SERIAL NO. 10/008,270 GROUP: Unknown

U.S. PATENT DOCUMENTS

EXAM. INITIALS	REF. DES.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
JSP	A1	5,812,824	9/22/98	Dearth, et al.			
JSP	A2	5,732,247	3/24/98	Dearth, et al.			
JSP	A3	5,881,267	3/9/99	Dearth, et al.			
JSP	A4	5,848,236	12/8/98	Dearth, et al.			
JSP	A5	6,031,987	2/29/00	Damani, et al.			
JSP	A6	5,910,903	6/8/99	Feinberg, et al.			
JSP	A7	5,850,345	12/15/98	Son			
JSP	A8	6,053,947	4/25/00	Parson			
JSP	A9	5,870,585	2/9/99	Stapleton			
JSP	A10	5,751,941	5/12/98	Hinds, et al.			
JSP	A11	5,634,010	5/27/97	Ciscon, et al.			
JSP	A12	6,117,181	9/12/00	Dearth, et al.			
JSP	A13	5,519,848	5/21/96	Wloka, et al.			
JSP	A14	5,442,772	8/15/95	Childs, et al.			
JSP	A15	5,339,435	8/19/94	Lukin, et al.			
JSP	A16	4,456,994	6/26/84	Segarra			
JSP	A17	5,625,580	4/29/97	Read, et al.			
JSP	A18	5,715,184	2/3/98	Tyler, et al.			
JSP	A19	5,794,005	8/11/98	Steinman			
JSP	A20	5,907,695	5/25/99	Dearth			
JSP	A21	4,821,173	4/11/89	Young, et al.			
JSP	A22	4,937,173	6/26/90	Kanda, et al.			
JSP	A23	5,185,865	2/9/93	Pugh			
JSP	A24	5,327,361	7/5/94	Long, et al.			
JSP	A25	5,455,928	10/3/95	Herlitz			
JSP	A26	6,345,242	2/5/02	Dearth, et al.			

EXAMINER: [signature] DATE CONSIDERED: 2/28/2005

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OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

JSP	A28	"Rule Base Driven Conversion of an Object Oriented Design Structure Into Standard Hardware Description Languages," Verschueren, A.C., IEEE Xplore, appears in Euromicro Conference, 1998, Proceedings. 24th, vol. 1, August 25, 1998, pages 42-45.
	A29	"Modeling Communication with Objective VHDL," Putzke, et al., IEEE Xplore, appears in Verilog HDL Conference and VHDL International Use Forum, 1998, IVC/VIUF, Proceedings., 1998 International, March 16, 1998, pages 83-89.
	A30	"A Procedural Language Interface for VHDL and its Typical Applications," Martinolle, et al., IEEE Xplore, appears in Verilog HDL Conference and VHDL International Use Forum, 1998, IVC/VIUF, Proceedings., 1998 International, March 16, 1998, pages 32-38.
	A31	"The Verilog Procedural Interface for the Verilog Hardware Description Language," Dawson, et al., IEEE Xplore, appears in Verilog HDL Conference, 1996, Proceedings., 1996 International, February 26, 1996, pages 17-23.
	A32	"An Integrated Environment for HDL Verification," York, et al., IEEE Xplore, appears in Verilog HDL Conference, 1995, Proceedings., 1995 International, March 27, 1995, pages 9-18.
	A33	"The PowerPC 603 C++ Verilog Interface Model," Voith, R.P., IEEE Xplore, appears in Compcon Spring '94, Digest of Papters, Feb. 28, 1994, pages 337-340.
	A34	"Networked Object Oriented Verification with C++ and Verilog, Dearth, et al., IEEE, XP-002144328, 1998, 4 pages.
	A35	Patent Abstracts of Japan, publication no. 10326835, published December 8, 1998.
	A36	Patent Abstracts of Japan, publication no. 10049560, published February 20, 1998.
	A37	Patent Abstracts of Japan, publication no. 10340283, published December 22, 1998.
	A38	Patent Abstracts of Japan, publication no. 07254008, published October 3, 1995.
	A39	"Multiprocessing Verilog Simulator Exploits the Parallel Nature of HDLs." Lisa Maliniak, Electronic Design, Abstract, May 30, 1994, 1 page.
	A40	"It's A Multithreaded World, Part I," Charles J. Northrup, BYTE, May 1992, 7 pages.
	A41	"It's a Multithreaded World, Part 2," Charles J. Northrup, BYTE, June 1992, pp. 351-356.
	A42	"Weaving a Thread," Shashi Prasad, BYTE, October 1995, pp. 173-174.
	A43	"Making Sense of Collaborative Computing," Mark Gibbs, Network World Collaboration, January 10, 1994, 4 pages.
	A44	"Parallel Logic Simulation of VLSI Systems," Bailey, et al., ACM Computing Surveys, Vol. 26, No. 3, September 1994, pp. 255-294.
	A45	"Multithreaded Languages for Scientific and Technical Computing," Cherri M. Pancake, Proceedings of the IEEE, Vol. 81, No. 2, February 1993, pp. 288-304.
JSP	A46	"Distributed Simulation Architecture, SW Environment, Enterprise Server Products," Purdue EE400 Presentation by Freyensee and Frankel, November 9, 2000, 13 pages.

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OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

JSP	A47	"BNF and EBNF: What Are They And How Do They Work?," Lars Marius Garshol, October 12, 1999, pp. 1-10.
JSP	A48	"VCK: Verilog-C Kernel," Testbench Automation, Distributed by Verilog Simulation, Hardware-Software Co-verification, 2001 Avery Design Systems, Inc., 8 pages.
JSP	A49	"Principles of Verilog PLI," Swapnajit Mittra, Silicon Graphics Incorporated, 1999, 10 pages.
JSP	A50	"IEEE Standard Hardware Description Language Based on the Verilog® Hardware Description Language," IEEE, December 12, 1995, 8 pages.
JSP	A51	"OpenVera 1.0, Language Reference Manual," Version 1.0, March 2001, pp. 4-1 to 4-34, pp. 5-1 to 5-32, 6-1 to 6-22, 7-1 to 7-24, 11-1 to 11-50, 12-1 to 12-8, 13-1 to 13-14, 14-1 to 14-20, 15-1 to 15-118.
JSP	A52	"VLSI Designe of a Bust Arbitration Module for the 68000 Series of Microprocessors," Ososanya, et al., IEEE, 1994, pp. 398-402.
JSP	A53	"A VHDL Standard Package for Logic Modeling," David R. Coelho, IEEE Design & Test of Computers, Vol. 7, Issue 3, June 1990, pp. 25-32
JSP	A54	"Corrected Settling Time of the Distributed Parallel Arbiter," M.M. Taub, PhD., IEEE Proceedings, Part E: Computers & Digitals, Vol. 139, Issue 4, July 1992, pp. 348-354.

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c. ☐ after the mailing date of a final Office Action or a Notice of Allowance and prior to payment of the issue fee, and thus: the certification of paragraph 2 below is provided and a fee of $180.00 is enclosed.

2. It is hereby certified:

☐ that each item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the Statement, or

☐ that no item of information contained in the Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to the knowledge of the person signing the certification after making reasonable inquiry, was known to any individual designated in § 1.56 (c) more than three months prior to the filing of the Statement.

3. ☒ Consideration of the following additional information (including any co-pending or abandoned U.S. applications, prior uses and/or sales, etc.) is requested:

All considered 2/28/2005 JSB

U.S. Patent Application Serial No. 10/008,643 (5181-98000)
U.S. Patent Application Serial No. 09/262,575 (5181-11900)
U.S. Patent Application Serial No. 10/010,572 (5181-97900)
U.S. Patent Application Serial No. 10,008,271 (5181-96500)
U.S. Patent Application Serial No. 10/008,255 (5181-96400)
U.S. Patent Application Serial No. 10/007,816 (5681-03600)
U.S. Patent Application Serial No. 10/008,155 (5181-96300)
U.S. Patent Application Serial No. 09/262,545 (5181-11802)

4. For each non-English language reference listed on the attached Form PTO-1449:

☐ reference is made to an English language translation submitted herewith, and/or

☐ reference is made to a foreign patent office search report (in the English language) submitted herewith, and/or

☐ reference is made to an English language translation of a foreign patent office search report submitted herewith, and/or

☐ reference is made to the concise explanation contained in the specification of the present application at page(s) _____, and/or

☐ reference is made to the concise explanation set forth below:

5. ☐ Applicant also offers the following comments for the Examiner's consideration:

6. ☐ Also enclosed is a copy of a foreign search report citing these references.